REMARKS

The Examiner has objected to the drawings because Figure 1 was not labeled "Prior Art". A replacement sheet labeling Figure 1 as "Prior Art" was submitted December 7, 2006, and applicant trusts that the objection to the drawings will be withdrawn.

The Examiner has objected to the specification because the abstract was incomplete and because he cannot find support for some of the limitations of Claims 3, 17 and 21. The error in the abstract is being corrected, and statements are being added to the specification to support Claims 3, 17 and 21. No new matter is being added, and with these amendments, applicant trusts that the objection to the specification will be withdrawn.

Claims 4, 18 and 24 have been rejected under 35 U.S.C. §112 as being indefinite because of language which deleted from them in the Amendment filed July 10, 2006. Based upon the telephone conference between applicant's attorney and Examiner Mondt on December 7, it is applicant's understanding that the issues addressed in the rejection have been resolved and that the inclusion of the rejection in the latest action was an error on the part of the Examiner.

In order to move the application along, the terminology to which the Examiner has objected ("relatively thin", "relatively thick", "relatively high" and "relatively low") is being eliminated from Claims 3, 9, 10, 11, 17 and 21 even though applicant still believes it was perfectly clear and proper. With this amendment, all of the formal issues should be resolved.

Claims 1 - 13 and 15 - 22 have now been rejected under 35 U.S. C. §103 as being unpatentable over Hsu et al. (U.S. 6,911,690) in view of either prior art admitted by applicant in combination with Chapman et al. (U.S. 6,118,161) or Sakui et al. (U.S. 6,411,548) in combination with Chapman et al. This is identical to the rejection previously made by the Examiner except for the addition of Claims 19 - 22 and the use of the background section of applicant's disclosure as prior art. Once again, the Examiner has failed to include Claim 24 in the statement of the rejection even though it is included in the discussion.

In making this rejection, the Examiner continues to misconstrue and mischaracterize what is actually found in the references, and he continues to try to combine selected elements from the different references (and now from applicant's own disclosure) when there is no basis for doing so.

The array shown in Hsu et al. has a string of memory cell structures 132a - 132d formed between drain and source regions 124, 126. There are no bit lines, bit line diffusions or bit line contacts, as in applicant's invention, nor is there any overlapping or partial overlapping of a source region by a select gate. In that regard, applicant would draw the Examiner's attention to the paragraph bridging Columns 5 and 6 of Hsu et al., which makes it quite clear that region 124 is a drain region and not a bit line diffusion. If the Examiner has any support at all for characterizing drain region 124 as a bit line diffusion, he is requested to provide it.

Moreover, notwithstanding the Examiner's arguments about the inherency of bit lines, bit line contacts and bit line diffusions, nowhere in the prior art is there any suggestion of bit line and source diffusions at opposite ends of a row of alternating stacked gates and select gates with no other diffusions in the active area between the bit line diffusion and the source region. Even if such elements were inherent in the device of Hsu et al., where would they be? Is the Examiner going to change the source region or the drain region of Hsu et al. to a bit line diffusion and then add a bit and a bit line contact? If so, where is the motivation for doing so, and how does the Examiner know that the resulting device would work?

Sakui et al. and Figure 1 of applicant's disclosure are cited as showing a select gate partially overlapping a source region, a feature the Examiner acknowledges is not found in Hsu et al. However, neither Sakui et al. nor the prior art discussed in the background section of applicant's disclosure even remotely suggests a select gate which partially overlaps a source region in a memory cell array having the other elements of applicant's invention.

Chapman et al. is once again cited as showing that it is well known that a gate should overlap with a source for low series resistance and consistent high performance. However, that statement was made in the specific context of a MOSFET, not a NAND flash memory cell array, and Chapman et al. certainly does not suggest a select gate

which overlaps a source diffusion in a memory cell array having the other features of applicant's invention.

Claim 1 distinguishes over the combined teachings of the references in calling for a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row at least partially overlapping the source region, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion. As discussed above, the references fail to teach or even suggest a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region. They likewise fail to show or suggest a row of stacked gates and select gates with the last select gate in the row at least partially overlapping the source region.

Claims 2 - 13 depend from Claim 1 and distinguish over the references for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 2 specifies that the stacked gates and the select gates are self-aligned relative to each other.

Claim 3 further distinguishes in calling for a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first dielectric and the second dielectric. As the Examiner has acknowledged, this relationship is not taught by Hsu et al. or the other references. Hsu et al. is silent as to the relative thickness of the different dielectrics, and there is no basis for the Examiner's argument that cost considerations mandate that two of the dielectric layers should be thicker than the other.

Claim 4 further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and

the floating gates and between the control gates and the floating gates. In arguing that any non-zero inter-gate capacitance implies a voltage coupling between the gates, the Examiner has failed to consider the clear language of the claim which defines the control gates and the select gates as surrounding the floating gates.

Claim 5 further specifies that erase paths extend from the floating gates, through tunnel oxides below the floating gates to channel regions in the substrate, and voltage is coupled to the floating gates both from the control gates and from the select gates.

Claim 6 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region.

Claims 7 - 12 further distinguish over the references in calling for the application of specific voltages to different elements in the memory array.

In that regard, Claim 7 specifies that program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and the select gate on the bit line side of the stacked gates in a selected cell is biased at a lower voltage than the other select gates in the row to control channel current for efficient hot carrier injection during a program operation.

Claim 8 specifies that the select gates in unselected cells are biased at a voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source region. Here again, the Examiner has erred in ignoring a specific structural limitation as to the manner in which specific elements are biased. The intended use or functional language argument is the same one that the Examiner made in connection with the rejection of Claim 7, and it is fallacious for the same reasons.

Claim 9 specifies that the bit line for a row containing a selected cell to be programmed is held at 0 volts, a first positive voltage is applied to a cell select gate for the selected cell, a voltage higher than the first positive voltage is applied to the source region at the end of the row in which the selected cell is located, a voltage higher than the first positive voltage is applied to the control gate in the selected cell, a voltage higher than the first positive voltage is applied to the select gates for unselected cells, and a voltage higher than the first positive voltage is applied to the control gates in the

unselected cells. Here again, the Examiner has failed to give patentable weight to the specific limitations which distinguish over the references.

Claim 10 specifies that an erase path is formed by a first negative voltage on the control gates and a negative voltage smaller than the first negative voltage on the select gates, with the bit line diffusion, the source region and the P-well at 0 volts.

Claim 11 specifies that an erase path is formed by a first negative voltage on the control gates and negative voltage smaller than the first negative voltage on the select gates, with the active area at a positive voltage and the bit line diffusion and the source region floating.

Claim 12 specifies that a read path is formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells, with the common source at 0 volts, the bit line diffusion at 1 - 3 volts, and the control gate of the selected cell biased at 0 – 1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state.

The Examiner has taken the position that biasing and the application of other voltages are "intended use" or functional limitations to which no patentable weight is given. In so doing, he has overlooked the fact that the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode and the application of specific and/or relative voltages to specific elements are indeed structural limitations. Although they may define the structure as it is in use, they are nevertheless structural in nature and, therefore, entitled to patentable weight.

Claim 13 further calls for an erase path which can erase the whole cell array simultaneously and a program path which is single cell selectable.

Claim 15 distinguishes over the references in calling for a bit line diffusion and a source diffusion in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source diffusion, with each of the stacked gates having a control gate positioned above a floating gate and the last select gate in the row being directly above the source diffusion, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion. As noted above, the references fail to teach or even suggest a bit line diffusion and a source region in the active area of a substrate with no

other diffusions in the active area between the bit line diffusion and the source region. They likewise fail to show or suggest a row of stacked gates and select gates with the last select gate in the row being directly above the source region. , and the Examiner is mistaken in suggesting that this structure is shown in Sakui et al.

Claims 16 - 18 depend from Claim 15 and distinguish over the references for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 16 specifies that the select gates are self-aligned to the control and floating gates.

Claim 17, like Claim 3, further distinguishes in calling for a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first and second dielectrics.

Claim 18, like Claim 4, further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

Claim 19 distinguishes over the references in calling for a substrate having an active area, bit line diffusions and source diffusions spaced alternately in the active area with no other diffusions between them, a plurality of stacked gates and select gates arranged alternately in rows between the bit line diffusions and the source diffusions, with each of the stacked gates having a control gate positioned above a floating gate and the last select gates in each of the rows at least partially overlapping the source diffusions between the rows, a bit line above each row, and bit line contacts interconnecting the bit lines and the bit line diffusions. As discussed above, the references taken individually or collectively fail to disclose or even remotely suggest a memory cell array having these features.

Claims 20 - 22 depend from Claim 21 and are directed to patentable subject matter for the same reasons as their parent claim. In addition, they call for additional features which are not found in or suggested by the references.

Claim 20 specifies that the floating gate and the control gate in each of the stacked gates are self-aligned with respect to each other.

Claim 21, like Claim 3 and Claim 17, further distinguishes in calling for a tunnel oxide between the floating gates and the substrate, a first dielectric between the floating gates and the select gates, and a second dielectric between the floating gates and the control gates, with the tunnel oxide being thinner than the first and second dielectrics.

Claim 22, like Claim 4 and Claim 17, further distinguishes in specifying that the control gates and the select gates surround the floating gates in a manner which provides inter-gate capacitances between the select gates and the floating gates and between the control gates and the floating gates which are large enough to couple voltages between the select gates and the floating gates and between the control gates and the floating gates.

Claim 24 distinguishes over the references in calling for a bit line diffusion and a source region in the active area of a substrate with no other diffusions in the active area between the bit line diffusion and the source region, a plurality of stacked gates and select gates arranged alternately in a row above the active area between the bit line diffusion and the source region, with each of the stacked gates having a control gate and a floating gate with self-aligned sides adjacent to the select gates, erase paths between the floating gates and channel regions in the active area beneath the stacked gates, and voltage coupling from the control gates and the select gates to the floating gates.

With this amendment, it is respectfully submitted that Claims 1 - 13, 15 - 22, and 24 are all directed to patentable subject matter and that the application is in condition for allowance.

The Commissioner is authorized to charge any fees required in this matter, including extension fees, to Deposit Account 50-2975, Order No. A-75000.

Respectfully submitted,

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